SOLID-STATE LIGHTING: LAMPS, CHIPS AND MATERIALS FOR TOMORROW

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1 Introduction

Dramatic changes are unfolding in lighting technology. Semiconductor-based solid-state lighting (SSL), until recently associated mainly with simple indicator lamps in electronics and toys, have become as bright and efficient as incandescent bulbs, at nearly all visible wavelengths. They have already begun to displace incandescent bulbs in many applications, particularly those requiring durability, compactness, cool operation and/or directionality (e.g., traffic, automotive, display, and architectural/directed-area lighting).

Further major improvements in this technology are believed achievable. External electrical-to-optical energy conversion efficiencies exceeding 50% have been achieved in infrared[1] and deep-red[2] light emitting devices. If similar efficiencies are achieved across the visible spectrum, the result would be the holy grail of lighting: a 150-200lm/W white light source two times more efficient than fluorescent lamps, and ten times more efficient than incandescent lamps.

This new white light source would change the way we live, and the way we consume energy. The human visual experience would be enhanced, through lights whose intensity and color temperature are independently tunable while maintaining high efficiency. In the long term, worldwide electricity consumption for lighting could decrease by more than 50%, and total electricity consumption could decrease by more than 10%.[3]

The aim of this article is twofold.

First, we give a brief historical and forward-looking overview of conventional and SSL lighting technologies. We focus on SSL technology based on inorganic light-emitting diodes (SSL-LEDs), rather than those based on organic light-emitting diodes (SSL-OLEDs), as SSL-LED technology is more advanced and more likely to be first to enter general illumination applications.

Second, we describe some of the simplest but most important lamp, chip and materials design choices that will need to be made. We especially focus on the constraints imposed on those design choices if SSL-LED technology is to fulfill its promise for general illumination. Note that quantifying these constraints depends to some extent on physical models and assumptions about the relationship between design and performance. Hence, the constraints can be viewed as providing interim guidance to lamp, chip and materials technologists, while stimulating development of improved physical models and assumptions by semiconductor scientists.

2 Condensed History of Lighting

Lighting technologies are substitutes for sunlight in the 425-675 nm spectral region where sunlight is most concentrated and to which the human eye has evolved to be most sensitive. The history of lighting can be viewed as the development of increasingly efficient technologies for creating visible light inside, but not wasted light outside, of that spectral region.

A 200-year perspective on that history is shown in **Figure 1**.[4] The left axis indicates luminous efficacy, in units of lumens (a measure of light which factors in the human visual response to

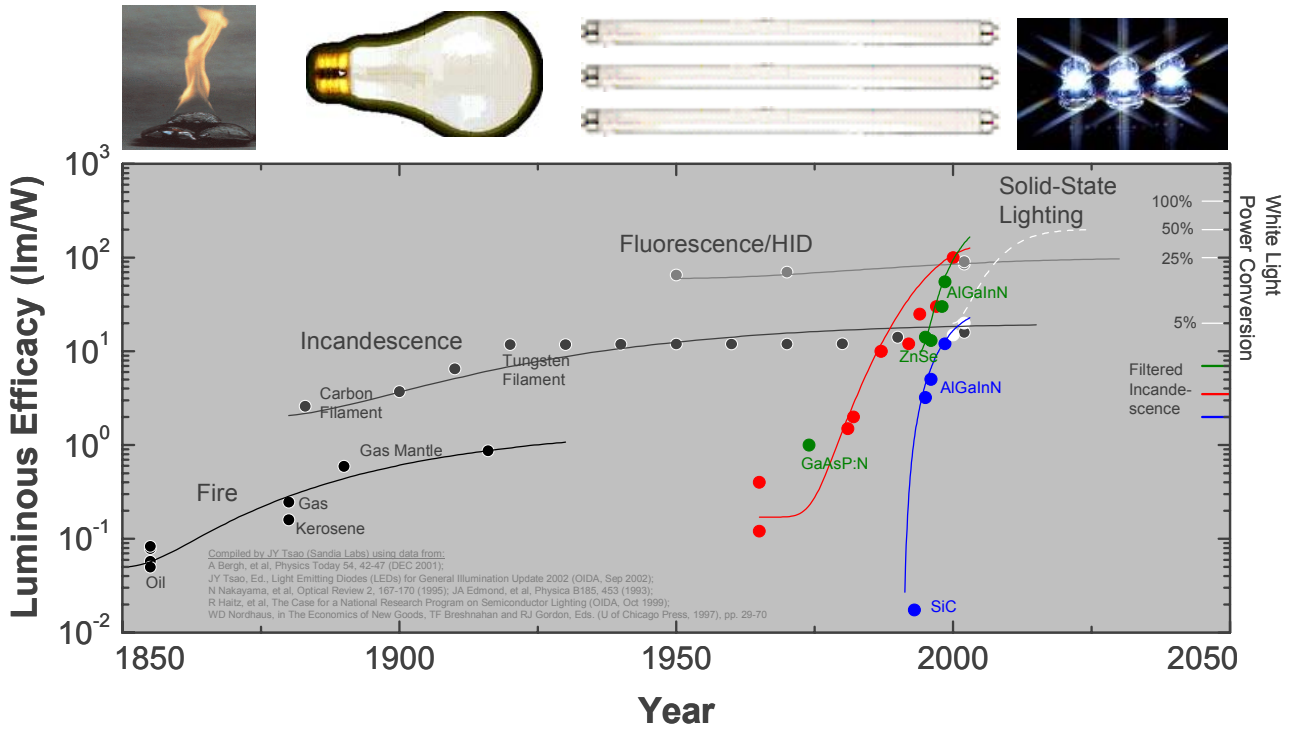

Figure 1: 200-year evolution of luminous efficacy for various lighting technologies.

various wavelengths) per watt. The right axis indicates the corresponding power-conversion efficiency for a tri-LED-color white light source with moderate color rendering (CRI=80) and relatively warm color temperature (CCT=3900K). For such a source, 400lm/W would correspond to 100% power-conversion efficiency.[5]

The three traditional technologies are Fire; Incandescence; and Fluorescence and High-Intensity Discharges (HID). These three traditional technologies have all made significant progress over the past 200 years, but appear to be saturating at efficiencies in the 1-25% range.

A new, fourth technology is Solid-State Lighting. In principle, the technology is simple: electrons and holes are injected into a forward-biased semiconductor p-n junction; they recombine creating photons; the resulting photons are extracted from the chip; then the photons are either mixed with different-color photons from other LEDs, or are energy down-converted into a distribution of colors using phosphors or other down-conversion materials, with the colors chosen so as to create the appearance of white.

In practice, there are losses at every step of the way, and *efficiently* creating white light from semiconductor materials with band-gaps that span the visible spectrum is extremely challenging. Nevertheless, great strides are being made, and SSL-LED technology is currently on a very rapid improvement curve, particularly the monochrome lamps in the red, green and blue[6] on which it is based.

A possible future scenario for white SSL-LED lamps is shown, in the dashed white lines in **Figure 1**, for which power-conversion efficiency rises to 50% by the year 2020. This scenario, envisioned in a recent Roadmap[7] for SSL-LED technology, is shown in more detail in **Table 1**. Note that this scenario was developed under the assumption that significant national investment, beginning in 2002, be directed towards key science and technology challenges. The scenario is likely to be different under different national investment assumptions. Nevertheless, the scenario itself gives an idea of the ultimate performances that can be expected from this technology.

	SSL-LED 2002	SSL-LED 2007	SSL-LED 2012	SSL-LED 2020	Incandescent	Fluorescent	HID
LAMP TARGETS							
Luminous Efficacy (lm/W)	20	75	150	200	16	85	90
Lifetime (hr)	20,000	20,000	100,000	100,000	1,000	10,000	20,000
Flux (lm/lamp)	25	200	1,000	1,500	1,200	3,400	36,000
Input Power (W/lamp)	1.3	2.7	6.7	7.5	75.0	40.0	400.0
Lamp Cost (in $/klm)	200.0	20.0	5.0	2.0	0.4	1.5	1.0
Lamp Cost (in $/lamp)	5.0	4.0	5.0	3.0	0.5	5.0	35.0
Color Rendering Index (CRI)	70	80	80	80	100	75	80
DERIVED LAMP COSTS							
Capital Cost [$/Mlmh]	12.00	1.25	0.30	0.13	1.25	0.18	0.05
Operating Cost [$/Mlmh]	3.50	0.93	0.47	0.35	4.38	0.82	0.78
Ownership Cost [$/Mlmh]	15.50	2.18	0.77	0.48	5.63	1.00	0.83

Table 1: Roadmap Scenario for SSL-LED Technology, along with Comparisons to Traditional Lighting Technologies.

The top half of the Table shows scenarios for the various lamp cost and performance parameters: luminous efficacy, in lm/W; lifetime, in hours; flux per lamp, in lm/lamp; input power to the lamp, in Watts/lamp or W/lamp; cost to purchase a lamp, in $/klm; cost to purchase a lamp in $/lamp; and finally color rendering index, or CRI, a measure of the quality of the white light.

The bottom half of the Table shows derived lamp costs to the consumer. The capital cost is the cost (per Mlm) to purchase the bulb or lamp, plus the labor cost to replace the bulb or lamp when it burns out, both amortized over its lifetime (up to a maximum of 20,000 hours). The operating cost is the cost (per Mlm-hour or Mlmh) to run a light bulb or lamp – basically the ratio between the cost of the fuel and the luminous efficacy.[8] The life-ownership or ownership cost is the sum of the capital and operating costs. The units for all three are $/Mlmh.

The ownership cost can be viewed as a single figure-of-merit for the economic case for SSL-LEDs. One can see that, if the scenario comes to pass, the ownership cost of SSL-LEDs will be lower than that of Incandescence by 2007, lower than those of Fluorescence and HIDs by 2012, and much lower than all traditional lighting by 2020.

This scenario is aggressive, and it is by no means assured that it will come to pass. SSL-LED technology, though advancing rapidly, is still in its infancy, particularly with respect to general illumination applications. Even very basic design choices are still being debated, and it is not yet clear which choices will best balance what is technologically possible with what the market prefers.

In the remainder of this article, we discuss some of these design choices, for the lamp, for the chip "light engine" that will be the heart of the lamp, and for the semiconductor materials that the chip will be made from. Throughout, we assume that these design choices must be consistent with the long-term Roadmap scenario, in order to clarify the challenges associated with that scenario.

3 Lamp Design Choices

For the lamp, illustrated in **Figure 2**, the major design choice is between: phosphor down-conversion or color mixing (along with hybrids between these two extremes). Phosphor down-conversion involves using a UV/purple LED to excite phosphors that emit wavelength-down-converted RGB white light. Color-mixing involves mixing colors from multiple LEDs to create RGB white light.

Phosphor down conversion, because of its low system complexity, and because UV/purple LEDs and associated phosphors already exist, albeit with improvements to be desired, is the clear current design choice.

In the long run, however, color mixing is likely to be more efficient, because it incurs no down-conversion losses. And, it is important to note, as efficiency is increased, both the operating and capital costs discussed in **Section 2** decrease. Hence, higher efficiency is critical not just because it may lead to savings in electricity consumption, but because it will reduce the capital

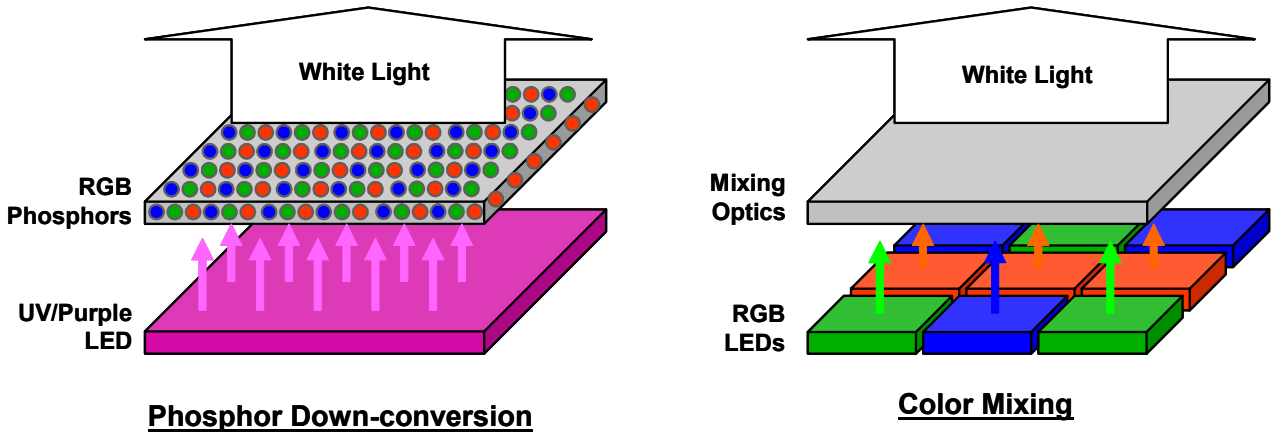

Figure 2: Phosphor down-conversion and color mixing approaches to SSL-LED lamps.

cost associated with purchasing a given number of lumens.

Hence, lower ownership cost will favor color mixing, provided it is technologically possible. Currently, though, it is not -- reasonably efficient LEDs currently exist only in the purple/blue and red portions of the spectrum. Thus, one of the outstanding challenges in SSL-LED science and technology is efficient LEDs in the green/yellow/orange, where the human eye is most sensitive.

4 Chip Design Choices

For the chip "light engine" that will be at the heart of the lamp, one of the simplest but most important design choices has to do with the size of the chip. The constraints on this design choice can be quantified by considering the characteristics of the semiconductor chip, illustrated in **Figure 3**, necessary for the Roadmap scenario to come to pass:

- First, the chip must produce 1.5klm of white light – roughly the output of a 100W incandescent light bulb.
- Second, the chip must have a luminous efficacy of 200lm/W. The ratio between the 1.5klm light output and the 200lm/W luminous efficacy gives 7.5W of input power. As mentioned in Section 2, a 200lm/W luminous efficacy is approximately equivalent, for a reasonable CRI, to a power conversion efficiency of 50%. Hence, half of the 7.5W of input power goes into white light generation; the other half is lost and must be sunk by the heat sink.
- Third, the capital cost of the light must be roughly \$3 to the consumer per 1.5klm lamp. Assuming a factor 2x for wholesale-to-retail mark-up, and a factor 2x due to packaging cost, we can estimate that the chip must cost \$3 divided by 4x, or 75 cents, to purchase.

All together, the chip must cost 75 cents to purchase, must be driven by 7.5W, producing 3.75W of white light and sinking 3.75W of waste heat. Note that the cost to manufacture the chip may be yet another factor 2x lower than this, to allow for profits and mark-up by the chip manufacturer.

Given these overall chip characteristics, we can now ask: what are the cost and performance trade-offs that determine how large the chip can be? Some of the most important of these trade-offs are illustrated in the series of four graphs of **Figure 4**, all having chip area as a common y-axis.

4.1 Chip Areal Cost

The first trade-off, illustrated in **Figure 4D**, is that between the areal cost of the chip (in \$/cm^2) and the area of the chip. For a fixed chip cost of \$0.75, the chip areal cost c_{chip} must scale inversely as chip area A_{chip}:

$$c_{chip}(\$/cm^2) = \frac{0.75\$}{A_{chip}(cm^2)}. \qquad [1]$$

Two extremes can be imagined.

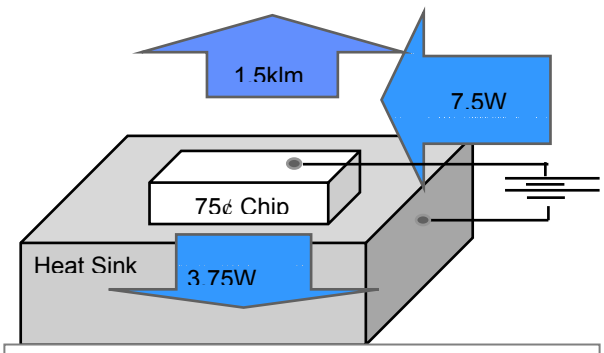

Figure 3: Geometry of SSL chip.

One extreme is low in cost: what one might call the red LED scenario, because AlGaInP/GaAs-based high-brightness red LEDs, for which unpackaged chips cost of the order \$30/cm^2 to purchase,[9] are a relatively inexpensive compound semiconductor technology. If GaN-based LEDS (or lasers) with the targeted performance were this inexpensive, the chip area could be as large as 2.5mm^2.

The other extreme is high in cost: what one might call the high-power laser scenario, because AlGaInAs/GaAs-based high-power semiconductor lasers, for which unpackaged chips cost of the order \$300/cm^2 to purchase,[10] are a relatively expensive compound semiconductor technology. If GaN-based LEDs (or lasers) with the targeted performance were this expensive, the chip area would in turn need to be as small as 0.25mm^2.

Note that two other points of reference for semiconductor chip areal costs are: silicon integrated circuits, for which unpackaged chips cost approximately \$5-15/cm^2 to purchase;[11] and state-of-the-art triple-junction compound-semiconductor solar cells, for which unpackaged chips cost approximately \$5-15/cm^2 to purchase.[12] These chips cost even less (per cm^2) to purchase than the low-cost extreme discussed above, and provide some support for the feasibility of the low-cost extreme. However, they are based on technologies sufficiently different from SSL that cost comparisons are difficult. In particular, neither technology is complicated by a need for efficient extraction of light from high-refractive-index semiconductors into low-refractive-index air. This complication may require relatively expensive chip-level (rather than wafer-level) fabrication processes for controlling optical modes and propagation, such as the facet cleaving/coating processes currently used to manufacture semiconductor lasers.

4.2 Chip Operating Power Density

The second trade-off, illustrated in **Figure 4C**, is that between the input power density to the chip p_{oper} (in W/cm^2) and the area A_{chip} of the chip. For a fixed operating input power of P_{oper}=7.5W, the chip operating input power density must scale inversely as chip area:

$$p_{oper}(W/cm^2) = \frac{7.5W}{A_{chip}(cm^2)}. \qquad [2]$$

At the low-cost large (2.5mm^2) area extreme, chip input power densities would need to be 300W/cm^2. At the high-cost small (0.25mm^2) area extreme, chip input power densities would need to be 3kW/cm^2. Though these power densities are high, they are comparable to those used to drive high-power IR diode lasers, and are in and of themselves not likely to be insurmountable challenges. Instead, it is the indirect effect, discussed next in **Section 4.3**, that such power densities will have on chip operating temperature that is likely to be a more significant challenge.

4.3 Chip Operating Temperature

The third trade-off, illustrated in **Figure 4A** and **Figure 4B**, is that between the operating temperature of the chip, T_{oper}, and the area of the chip.

Consider a disk-shaped chip mounted using thermal paste to a semi-infinite heat sink. Assume that the chip/paste combination has an area A_{chip}, thickness h_{chip}, and aspect ratio $\alpha=(4A_{chip}/\pi)^{0.5}/h_{chip}$. Such a chip/paste combination, generating heat then conducting it into a semi-infinite heat sink, will have a thermal resistance that scales [13] inversely as both the square root of its area, and the effective thermal conductivity κ_{eff} [14] of the chip/paste combination and heat sink:

$$R_T \cong \frac{1}{2\kappa_{eff}\sqrt{4A_{chip}/\pi}}. \qquad [3]$$

This equation, represented by the dashed curve, fits reasonably well the data points shown in Figure 2A for the thermal resistances of high-

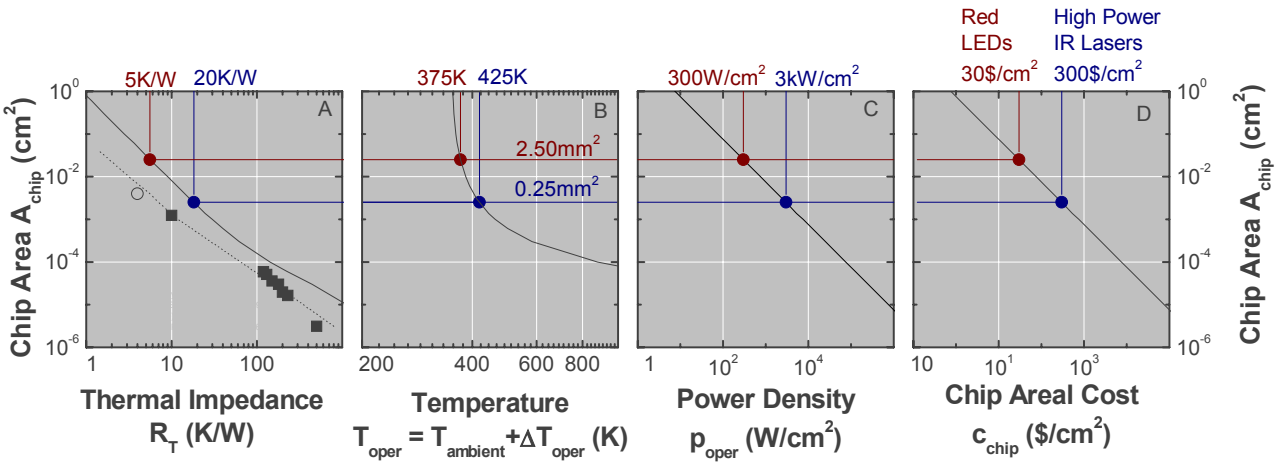

Figure 4: Scaling of chip thermal resistance, operating temperature and power density, and areal cost, with chip area.

power lasers with state-of-the-art active-area-down diamond-heat-sinking.[15]

To estimate the effective thermal resistance of SSL chips, we assume a similar chip/paste thickness, but chip/paste and heat-sink thermal conductivities a factor 4x lower, under the assumption that diamond heat-sinking will be too expensive.

As illustrated in **Figure 4B**, this means that, for a fixed power wasted into the heat sink, the chip operating temperature decreases as chip area increases. If the chip is large, its operating temperature will be low; if the chip is small, its operating temperature will be high. Assuming, in addition, that the combination of the heat sink and ambient temperature may itself be as high as 350K, we can write:

$$T_{oper} = 350K + R_T \cdot P_{oper} . \qquad [4]$$

At the inexpensive, red LED extreme with large, 2.5mm^2 chip areas, the operating temperature can be as low as 375K, only 75K above the normal room temperature of 300K. But at the expensive, high-power laser extreme with 0.25mm^2 chip areas, the operating temperature may need to be as high as 425K, 125K above normal room temperature. Though this operating temperature difference (from roughly 100C to 150C) may seem small, it can complicate significantly both chip performance and packaging.

4.4 Chip Area

Which of these two size extremes SSL technology will evolve towards is not yet clear. Certainly, in the past few years, there has been a short-term trend towards larger chips – from 0.25x0.25mm^2=0.0625mm^2 to 1x1mm^2=1mm^2 areas. This trend has been driven by a market need for higher light output per lamp, exacerbated by the low power-conversion efficiency of current technology.

In the long term, assuming power-conversion efficiency improves, chip size may depend on which aspect of efficiency proves more difficult to improve: radiative electron-hole recombination to generate light within the chip, or light extraction from the chip.

If the former is true, then non-radiative electron-hole recombination, which competes with radiative electron-hole recombination, is likely to be significant. If thermally activated, through carrier leakage out of intentional or unintentional composition fluctuations, then it is likely to be even more significant at higher operating temperatures. If so, larger chips that heat up less might be favored.

If the latter is true, then relatively expensive chip-level fabrication processes for controlling optical modes and propagation may be required. If so, smaller chips that are more expensive might be favored.

5 Materials Design Choices

For the semiconductor materials that the chip will be fabricated from, one of the simplest but most important design choices has to do with the quality of the materials that the chip will be fabricated from. This is an especially important design choice because the AlGaInN family of materials, likely to dominate SSL chips, is currently far more defective than more established semiconductor materials such as Si or GaAs.

Note that there are many possible measures of material quality. Here, we use dislocation density, under the assumption that dislocations have a stronger influence on important device performance characteristics than other kinds of defects. Also note that there are many possible choices of device performance characteristics. Here, we use internal radiative efficiency and lifetime, as these may be relatively easily connected back to the Roadmap scenario.

5.1 Internal Radiative Efficiency: GaN

Let us first consider internal radiative efficiency, as illustrated in **Figure 5B**. In order to achieve an overall power conversion efficiency of 50%, this efficiency must be near 100%, as it is likely that other losses, including those associated with current injection and light extraction, will be difficult to eliminate completely.

However, there is substantial evidence [16] indicating that, in GaN, radiative recombination is quenched in a capture zone around dislocations (illustrated as purple zones in the cartoon at the bottom of **Figure 5**). Hence, as dislocation density ρ_{disl} increases, internal radiative efficiency η_{int} decreases.

To first order, the capture zone may be viewed as having a radius on the order of the minority carrier diffusion length L_o. To second order, however, the minority carrier diffusion length itself depends on dislocation density. Hence, the dependence of internal radiative efficiency on dislocation density must in general be solved self-consistently.[17]

Here, we use a simple but approximate closed-form model[18]:

$$\eta_{\text{int}} = \frac{1}{1 + \pi^2 L_o^2 \rho_{disl}} . \qquad [5]$$

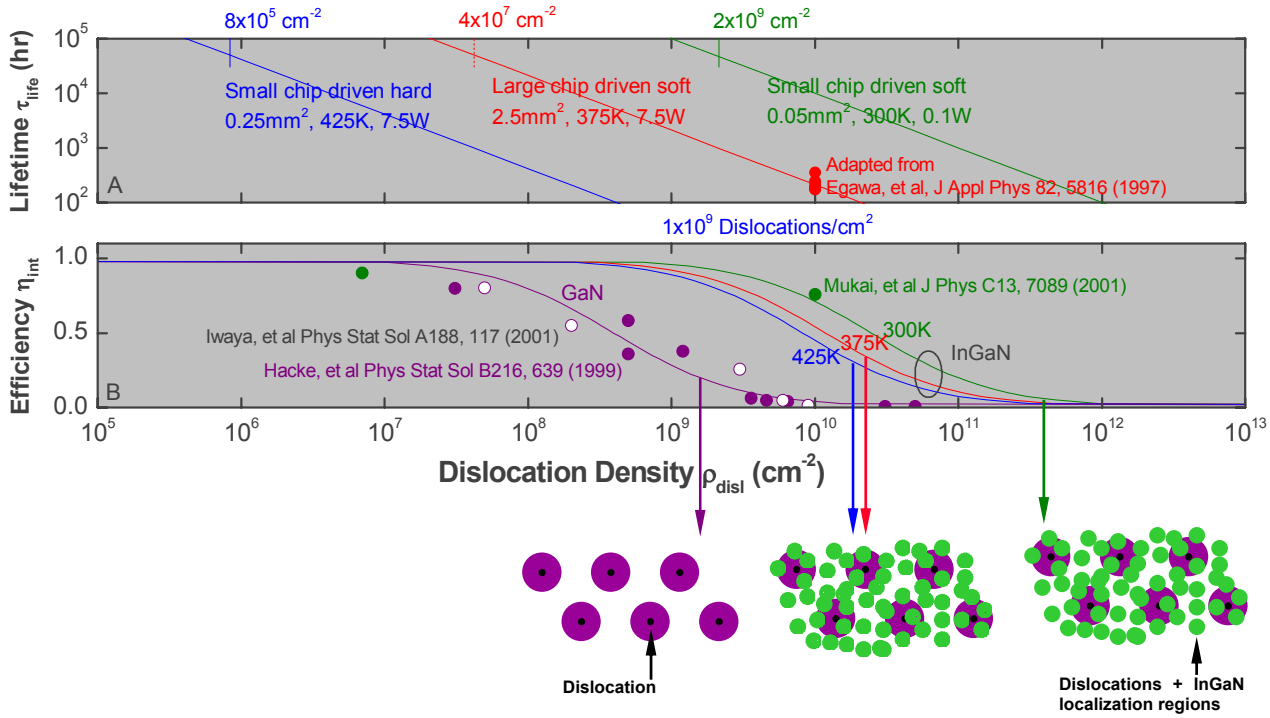

Figure 5: Scaling of chip efficiency and lifetime with dislocation density.

The dependence of internal radiative efficiency on dislocation density implied by this model is shown by the purple curve in **Figure 5B**, for a minority carrier diffusion length of $L_o = L_{o,GaN}$ = 160nm. This curve is a fit to the data points in purple.[19] The implication of this curve is that, for GaN, internal radiative efficiency begins to decrease noticeably at a dislocation density in the low 10^7/cm^2 range.

Note that the key parameter in Equation 5, the minority carrier diffusion length, depends on additional factors, such as carrier density and temperature. Hence, under some conditions (e.g., high current injection), the dependence of internal radiative efficiency on dislocation density can potentially be shifted to higher dislocation densities.

5.2 Internal Radiative Efficiency: InGaN

In InGaN, we assume that radiative recombination is, just as in GaN, quenched by dislocations. However, composition fluctuations and inhomogeneities (illustrated as the small green zones in the cartoon at the bottom of **Figure 5**), are thought to trap electron-hole pairs away from the dislocations.

To describe this trapping in an approximate way, here we assume that internal radiative efficiency still decreases with increasing dislocation density according to Equation 5. However, the effective capture radius now must be reduced due to trapping of electron-hole pairs away from the dislocations.

At low temperatures, we assume the trapping to be 100% efficient, and replace the capture radius with the spatial scale of the composition fluctuations, $L_o = L_{o,InGaN} \sim$ 5nm.

At higher temperatures, we assume that carriers occasionally escape from the composition fluctuations. The traps become "translucent," and at very high temperatures the capture radius must eventually increase back to that associated with pure GaN. To take this into account in a smooth though approximate way, we write:

$$L_o = L_{o,InGaN} + (L_{o,GaN} - L_{o,InGaN}) \cdot e^{-\delta E_{fluc}/kT} \quad [6]$$

Here, the transition from small to large effective capture radii is determined by the depth of the energy barriers δE_{fluc} associated with the composition fluctuations. The depth of the composition fluctuations depend on the average InGaN composition; for average InGaN compositions enabling emission at blue-green wavelengths, the fluctuations have been estimated to be $\delta E_{fluc} \sim$ 0.05-0.06eV.[20]

With these assumptions, the capture radius at room temperature (300K) is roughly $L_o \sim$ 20nm. Then, as illustrated by the green curve in **Figure 5B**, the decrease in internal radiative efficiency does not begin to be noticeable until dislocation densities are in the high 10^9/cm^2 range. As a rough comparison with experiment, we show data points in green from measurements[21] of InGaN radiative efficiency.

At the temperatures, 375K and 425K, associated with the two chip scenarios (low-cost large-area and high-cost small-area), the capture radii increase to roughly $l_o \sim$ 30nm and 35nm, respectively. As illustrated by the red and blue curves in **Figure 5B**, the associated decrease in radiative efficiency becomes noticeable at lower dislocation densities -- in the high 10^8/cm^2 range.

5.3 Implications of Internal Radiative Efficiency on Dislocation Density

All together, assuming the scaling relationships described in **Sections 5.1** and **5.2**, we can summarize the implications of dislocation density on internal radiative efficiency. For GaN, the necessary dislocation density appears to be in the low 10^7/cm^2 range. For InGaN, the necessary dislocation density appears to be in the high 10^8/cm^2 range.

Most importantly, both are within the range of current substrate and buffer layer technologies. The high 10^8/cm^2 range can be achieved in optimized single-growth buffers;[22] while the low 10^7/cm^2 range can be achieved in multiple-growth epitaxial lateral overgrowth buffers[23]. Hence, a tentative conclusion is that high internal radiative efficiency is not likely to require new substrate technologies with radically reduced dislocation densities.

5.4 Device Lifetime

Let us now consider device lifetime, illustrated in **Figure 5A**.

It is known that in many high-current-density compound-semiconductor-based optoelectronic

technologies, degradation is caused by non-radiative recombination at dislocations, which causes the dislocations to move, multiply, and eventually form dark-line defects that absorb light and reduce overall chip efficiencies.[24] Little is yet known about the physics of degradation in GaN and InGaN LEDs and lasers, and it is possible that resistance to dislocation motion is so high in these materials[25] that other mechanisms will dominate.

Here, however, we assume, as conjectured by Fang, et al., [26] that dislocation motion in the presence of high injected currents is a source of device degradation. Then, after all other processing-related failure mechanisms (e.g., ohmic-contact overheating) are eliminated, the dominant failure mechanism would be a dislocation-mediated mechanism similar to that of other compound-semiconductor-based optoelectronic devices. If so, device lifetime might scale inversely with both dislocation and current density, and be "lightly" thermally activated:

$$\tau_{life} = B \cdot \rho_{disl}^{-1} \cdot j_{curr}^{-1} \cdot e^{\Delta E / kT} . \qquad [7].$$

Then, through an analysis of data by Egawa et al.[27], we can estimate the parameters B and ΔE, and project the curves illustrated in **Figure 5A**.

The curve in green is the lifetime for a small chip driven fairly softly – this is roughly the past year's (2002) technology. For a dislocation density in the mid 10^9/cm^2 range, the lifetime projects out to 20,000 hours, which is roughly consistent with experience.

The curve in red is the lifetime for the large-chip scenario -- to achieve lifetimes of 50,000 hours, dislocation densities need to be less than $4x10^7$/cm^2. Superimposed over the curve in red is the data of Egawa, et al, scaled using Equation 7 to the current density (7.5W/[3Vx2.5mm^2]) and temperature (375K) associated with the large-chip scenario, to give an indication of the self-consistency of the data and fit.

The curve in blue is the lifetime for the small-chip scenario -- to achieve lifetimes of 50,000 hours, dislocation densities need to be less than $8x10^5$/cm^2.

Hence, if these projections are valid, the dislocation density necessary for long-lived GaN and InGaN chips is in the 10^6 to 10^8/cm^2 range, depending on whether the small or large chip scenario "wins." These dislocation densities are roughly one order of magnitude lower than those found, in **Sections 5.1** and **5.2**, necessary to ensure high internal radiative efficiency. Better data and better models are necessary, of course, but our interim conclusion is that device lifetime may constrain dislocation density more tightly than high internal radiative efficiency does.

Nevertheless, in the large-area chip scenario, the 10^8/cm^2 dislocation density required to ensure long-lived chips is high enough to be achievable using current substrate and buffer layer technologies. However, in the small-area chip scenario, the 10^6/cm^2 dislocation density required to ensure long-lived chips is low enough to require development of alternative substrate technologies. But it is high enough not to require development of thus-far-problematic melt-growth technologies capable of achieving dislocation densities less than 10^4/cm^2.

6 Conclusions

Solid-state lighting has tremendous potential, and the long-term lamp targets envisioned in the recent update to the U.S. SSL-LED Roadmap are intended to enable that potential.

Solid-state lighting is in its infancy, however, and many basic lamp, chip and materials design choices are being debated actively. However, these design choices are constrained if the technology is to achieve its potential in general white light illumination applications.

A first set of constraints takes the form of trade-offs between chip area, chip areal cost, and operating temperature and power density. Two extremes are possible: a large-area low-power-density low-areal-cost chip, and a small-area high-power-density high-areal-cost chip. The extreme that "wins" is conjectured to depend on which aspect of efficiency is more difficult to improve: radiative electron-hole recombination to generate light within the chip, or light extraction from the chip.

A second set of constraints takes the form of trade-offs between disclocation density, internal radiative efficiency, and device lifetime. The constraints on device lifetime appear to require lower dislocation densities than those on device

efficiency. In the large-area chip scenario, the required $10^8/cm^2$ dislocation densities can be achieved by current substrate and buffer technologies; but in the small-area chip scenario, the required $10^6/cm^2$ dislocation density may require development of alternative substrate technologies.

7 Acknowledgements

We acknowledge: the many contributors to the SSL-LED Roadmap Update 2002; Paul Martin (LumiLeds) and Mike Coltrin (Sandia), for their initial encouragement to go beyond the roadmap and develop "constrained" technical cost models such as described here; and Mary Crawford, George Craford, Hiroshi Amano, Mike Coltrin, Cesar Donolato, Jim Speck, Arpad Bergh and the Sandia Solid-State Lighting Team, managed by Jerry Simmons, Bob Biefeld and James Gee, for helpful comments and criticism.

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract DE-AC04-94AL85000.

8 Endnotes

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[3] J.Y. Tsao, "The U.S. LEDs for General Illumination Roadmap," Laser Focus World, S11-S14 (May 2003). Assuming 100% market penetration and 50% power conversion efficiency, the electricity savings in the U.S. projected out to the year 2025 would be roughly 525TW-hr/yr, or roughly $35B/yr, and the savings in C-equivalent emissions created during the generation of that electricity would be approximately 87Mtons. Worldwide, the figures are all about a factor of 3-4 higher. See also Navigant Consulting Inc., Energy Savings Potential of Solid State Lighting in General Illumination Applications (Building Technologies Program, Office of Energy Efficiency and Renewable Energy, U.S. Department of Energy, Nov 2003) for estimates that take into account time delays in market penetration.

[4] Data for this figure was compiled from A. Bergh, M.G. Craford, A. Duggal, and R. Haitz, "The promise and challenge of solid-state lighting," Physics Today **54**, 42-47 (Dec 2001); J. Edmond, H. Kong, and C. Carter, "Blue LEDs, UV Photodiodes and High-Temperature Rectifiers in 6H-SiC," Physica B: 7th Trieste ICTP-IUPAP Semiconductor Symposium **185**, 453-460 (1993); N. Nakayama, S. Kijima, S. Itoh, T. Ohata, A. Ishibashi, and Y. Mori, "High-Efficiency ZnCdSe/ZnSSe/ZnMgSSe Green Light-Emitting-Diodes," Optical Review **2**, 167-170 (1995); R. Haitz, F. Kish, J. Tsao, and J. Nelson, The Case for a National Research Program on Semiconductor Lighting (Optoelectronics Industry Development Association, Oct 1999); W.D. Nordhaus, "Do Real-Output and Real-Wage Measures Capture Reality? The History of Lighting Suggests Not," in T.F. Breshnahan and R. J. Gordon, Ed., The Economics of New Goods, 29-70 (The University of Chicago Press, Chicago, 1997).

[5] The luminous efficacy that corresponds to 100% power-conversion efficiency is less than 400lm/W for sources containing more colors, or having higher CRIs and CCTs.

[6] Note that only the left luminous efficacy, not the right power-conversion efficiency, axis should be applied to these monochrome LEDs. In the green, where the human eye is most sensitive, luminous efficacy would be as high as 683lm/W for a 100% power-conversion-efficiency LED.

[7] J.Y. Tsao, Ed., Light Emitting Diodes (LEDs) for General Illumination Update 2002 (Optoelectronics Industry Development Association, Sep 2002).

[8] The operating costs differ slightly from those of the SSL Roadmap 2002 due to a lower assumed cost of electricity ($0.07/kWh rather than $0.1/kWh) and a slightly lower 2002 luminous efficacy (20lm/W rather than 25lm/W).

[9] Low-medium-brightness LED lamp prices two years ago were of the order $0.1/lamp [R. Dixon, "High

Brightness LEDs," Compound Semiconductor Magazine, Jan 2000-Feb 2000)], and have continued to drop. Here, we use a conservative estimate of \$0.075/lamp for chips of area 0.25mmx0.25mm. Discounting a factor 4x for relatively simple packaging and for retail mark-up, the purchase price of unpackaged chips is then estimated to be on the order of (and likely somewhat less than) (\$0.075) x (¼) / $(0.25\text{mm})^2 \sim \$30/\text{cm}^2$.

[10] Power outputs of fully packaged high-power semiconductor diode laser bars are of the order 50W from areas about 10mmx1mm [H.G. Treusch, A. Ovtchinnikov, X. He, M. Kanskar, J. Mott, and S. Yang, "High-Brightness Semiconductor Laser Sources for Materials Processing: Stacking ; Beam Shaping ; and Bars," Ieee Journal of Selected Topics in Quantum Electronics **6**, 601-614 (Jul 2000-Aug 2000)]. Assuming a purchase price for such a fully packaged bar of \$6/W [D. Wolft, "Lasers and Light Sources: High-Power Diode Lasers," Photonics Spectra, Jan 2000)], then discounting a factor 10x for relatively sophisticated packaging and for retail mark-up, the purchase price of unpackaged chips is estimated to be on the order (\$6/W) x (1/10) x ($50\text{W}/0.1\text{cm}^2$) ~ $\$300/\text{cm}^2$.

[11] Blackwell, Jason, "Foundry wafer prices: Still hanging tough, but for how long?," Semiconductor Business News (Nov 6, 2001).

[12] J. M. Gee, "Unpublished Analysis of SSL 2020 Cost Targets," (Jun, 2001).

[13]Carslaw, H. S. and Jaeger, J. C., "Conduction of Heat in Solids," (Clarendon Press, Oxford, 59), p. 217.

[14] If the aspect ratio α >>1, then most of the heat flow is in the heat sink, and κ_{eff} approaches that of the heat sink material, κ_{sink}. If the aspect ratio α ~1, then much of the heat flow is in the chip/paste combination, and κ_{eff} approaches that of the chip/paste itself, κ_{chip}. To treat this in a rough way, we use the mathematical approximation

$$\frac{1}{\kappa_{eff}} \cong \frac{h_{chip}/\kappa_{chip} + \sqrt{4A_{chip}/\pi}/\kappa_{\sin k}}{h_{chip} + \sqrt{4A_{chip}/\pi}},$$

where the effective chip/paste thickness is h_{chip}~30μm, the chip/paste thermal conductivity is κ_{chip}~2W/(cmK), and the diamond heat-sink thermal conductivity is κ_{sink}~20W/(cmK).

[15] L.J. Mawst, A. Bhattacharya, J. Lopez, D. Botez, D.Z. Garbuzov, L. Demarco, J.C. Connolly, M. Jansen, F. Fang, and R.F. Nabiev, "8 W Continuous Wave Front-Facet Power From Broad-Waveguide Al-Free 980 nm Diode Lasers," Applied Physics Letters **69**, 1532-1534 (Sep 1996); M. Grabherr, M. Miller, R. Jager, R. Michalzik, U. Martin, H.J. Unold, and K.J. Ebeling, "High-Power VCSELs: Single Devices and Densely Packed 2-D Arrays," IEEE Journal of Selected Topics in Quantum Electronics **5**, 495-502 (May 1999-Jun 1999).

[16] S.D. Lester, F.A. Ponce, M.G. Craford, and D.A. Steigerwald, "High dislocation densities in high-efficiency GaN-based light-emitting diodes," Applied Physics Letters **66**, 1249 (Mar 1995); S.J. Rosner, E.C. Carr, M.J. Ludowise, G. Girolami, and H.I. Erikson, "Correlation of Cathodoluminescence Inhomogeneity With Microstructural Defects in Epitaxial GaN Grown by MetalorGaNic Chemical-Vapor Deposition," Applied Physics Letters **70**, 420-422 (Jan 1997); J.S. Speck and S.J. Rosner, "The role of threading dislocations in the physical properties of GaN and its alloys," Physica B **274**, 24-32 (Dec 1999). See, however, Y. Sun, O. Brandt, and K. Ploog, "Photoluminescence intensity of GaN films with widely varying dislocation density," Journal of Materials Research **18**, 1247-1250 (2003) for some recent contradictory results.

[17] C. Donolato, "Modeling the effect of dislocations on the minority carrier diffusion length of a semiconductor," Journal of Applied Physics **84**, 2656-2664 (Sep 1998).

[18] R.J. Roedel, A.R. Vonneida, R. Caruso, and L.R. Dawson, "Effect of dislocations in Ga1-xAlxAs-Si light emitting diodes," Journal of the Electrochemical Society **126**, 637-641 (1979).

[19] Note, though, that we are not aware of reliable measurements of the dependence of absolute radiative efficiency on dislocation density. Hence, the data points shown are two separate sets of measurements of relative radiative efficiency, where we have normalized the highest efficiency data points in each set, at relatively low dislocation densities in the range $\rho_{disl}=4\text{x}107\text{cm}^{-2}$, to the nearly saturated value of 0.8, an assumption consistent with that made in a more detailed analysis by S.Y. Karpov and Y.N. Makarov, "Dislocation Effect on Light Emission Efficiency in Gallium Nitride," Applied Physics Letters **81**, 4721-4723 (Dec 2002).

[20]V.E. Kudryashov, S.S. Mamakin, A.N. Turkin, A.E. Yunovich, A.N. Kovalev, and F.I. Manyakhin, "Luminescence Spectra and Efficiency of GaN-Based Quantum-Well Heterostructure Light Emitting Diodes:

Current and Voltage Dependence," Semiconductors **35**, 827-834 (2001).

[21]T. Mukai, S. Nagahama, N. Iwasa, M. Senoh, and T. Yamada, "Nitride Light-Emitting Diodes," Journal of Physics-Condensed Matter **13**, 7089-7098 (Aug 2001). We normalized the highest efficiency data point, at relatively low dislocation densities in the range $\rho_{disl}=1x10^7 cm^{-2}$, to the nearly saturated value of 0.9, a value slightly higher than the 0.8 assumed in **Section 5.1** for GaN, due to the lower experimental dislocation density.

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[27]T. Egawa, T. Jimbo, and M. Umeno, "Characteristics of InGaN/AlGaN Light-Emitting Diodes on Sapphire Substrates," Journal of Applied Physics **82**, 5816-5821 (Dec 1997). The degradation rates measured in this study can be fit reasonably well assuming a thermal resistance of 170K/W, in the range of what one might expect from Figure 1A for a conventionally-mounted chip of area $0.22x0.22mm^2$, and using values of $B = 2x10^8$ $(h/s)(C/cm^4)$ and $\Delta E = 0.45eV$.